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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/522,085	01/21/2005	Antonius Adrianus Maria Van Wel	NL02 0668 US	7580

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EXAMINER	
ELLIS, KEVIN L	
ART UNIT	**PAPER NUMBER**
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/522,085	VAN WEL, ANTONIUS ADRIANUS MARIA	
	Examiner	Art Unit	
	Kevin L. Ellis	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. Claims 1-8 are presented for examination.

Claim Rejections – 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-8 are rejected under 35 U.S.C. § 102(b) as being anticipated by Sakakibara et al., U.S. Patent 5,590,353.

A) As to claims 1 and 4, Sakakibara et al. discloses the invention as claimed. There is a method for transmitting a vector in a computer system comprising a processor (see Fig 1), a multi-port memory (Fig 1 Ref 220), passing a base memory address to an address configuration means (see Col 1 Lines 13-56 and Col 15 Line 15 to Col 16 Line 55; specifically Fig 5 Ref 191-1, see Col 15 Lines 30-65), defining a set of memory addresses by the address configuration means using the base memory address and a configuration instruction for configuring the address configuration means (see Col 15 Line 15 to Col 16 Line 55), transmitting the vector to/from the multi-port memory at one time using the set of memory addresses (see Col 15 Line 15 to Col 16 Line 55).

B) As to claims 2 and 5, the address configuration means does include a plurality of register files (see Fig 1 Ref 191, 192, 193, and 194).

C) As to claims 3 and 6, the configuration does include an offset (see Col 15 Line 30 to Col 16 Line 23).

D) As to claim 7, the multi-port memory and the address configuration means can be considered to be included in a "memory system" (see Fig 1).

E) As to claim 8, the limitations have been addressed with respect to claim 1 above. As for the computer program it is inherent that a "program" would be executed by Sakakibara et al. that would cause the addresses to be created that are provided to the multi-port memory.

4. Claims 1, 2, 4, 5, 7, and 8 are rejected under 35 U.S.C. § 102(b) as being anticipated by Duboc, U.S. Patent 6,463,518.

A) As to claims 1 and 4, Duboc discloses the invention as claimed. There is a method for transmitting a vector in a computer system comprising a processor (see Fig 2 Ref 12), a multi-port memory (Fig 2 Ref 14), passing a base memory address to an address configuration means (Fig 2 Ref 40 and Col 8 Lines 32-42), defining a set of memory addresses by the address configuration means using the base memory address and a configuration instruction for configuring the address configuration means (see Fig 4 and Col 8 Line 42 to Col 9 Line 65), transmitting the vector to/from the multi-port memory at one time using the set of memory addresses (see Col 6 Line 63 to Col 7 Line 43).

B) As to claims 2 and 5, the address configuration means does include a plurality of register files (see Fig 4).

C) As to claim 7, the multi-port memory and the address configuration means can be considered to be included in a "memory system" (see Fig 2).

D) As to claim 8, the limitations have been addressed with respect to claim 1 above. As for the computer program it is inherent that a "program" would be executed by Duboc that would cause the addresses to be created that are provided to the multi-port memory.

Response to Arguments

5. Applicant's arguments filed 12/28/06 have been fully considered but they are not persuasive. Sakakibara et al. discusses transferring the vector data in parrallel which would appear to read upon the newly added limitation of "at one time" (see Col 15 Lines 30-40). Duboc also accessed data in parallel (Col 7 Lines 15-18).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin L. Ellis whose telephone number is 571-272-4205. The examiner can normally be reached on weekdays from 6:00AM-2:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone numbers for the organization where this application or proceeding is assigned is 571-272-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Kevin L. Ellis
Primary Examiner
February 14, 2007